



## UV PROM Application Note 113 Programming and Verify Problems Programmer Recommendation

### GENERAL DESCRIPTION

#### Introduction

Certain device programmers do NOT follow the reference specifications for programming Cypress and QP Semiconductor 7C2xx series UV PROMS. In many cases the Cypress devices do verify as programmed but since the correct spec was NOT followed there is a very real risk that the devices may “lose” the program data and fail in the field.

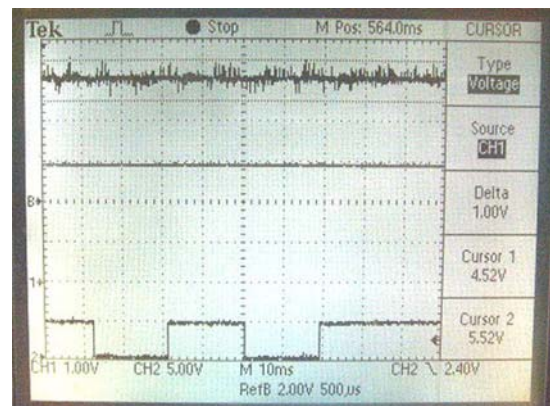
#### Observed Problems

QP has re-designed, re-engineered, and qualified the original Cypress brand UV PROMS. In field applications we found that certain programmers would not verify after programming. QP investigated one ALL-11 programmer and found the programming discrepancies, in particular, this ALL-11 does not follow the timing specifications of the programming spec nor does it apply the proper  $V_{CC}$  during the test sequences.

The principal problem we observed was that this ALL-11 had an insufficient over-programming pulse to ensure the cell was “full” during the programming cycle. An incompletely filled cell makes the equipment dangerous for long-term reliability of the programming. That is, the UV cell didn’t actually get “filled,” even though passing on the ALL-11. As we show in the following note, the UV PROM requires a 4X over-programming pulse to be certain that the cell is fully charged. The ALL-11 only provides a 1X over-programming pulse to supply the cell charge. So while the ALL-11 programs the cell faster it may do so at the expense of supplying a full charge to the cell.

#### Incorrect Supply Voltage

Fig.1 is a screen capture with detailed sampling of the  $V_{CC}$  level while the Verify pulse is active. This zoom-in is at the “read all words” portion of the ALL-11 test sequence. From the measurements on the screen one can observe that the  $V_{CC}$  level at the final verify is at 5V. In the image two lines (cursors) are placed above and below Ch1 of the screen capture. The spec calls for the  $V_{CC}$  voltage to be applied at 4.5V and then at 5.5V as shown with the lines. However one can see that  $V_{CC}$  is kept at 5V throughout the test sequence. From our observations we see that the ALL-11 is not performing the tests per the specification.

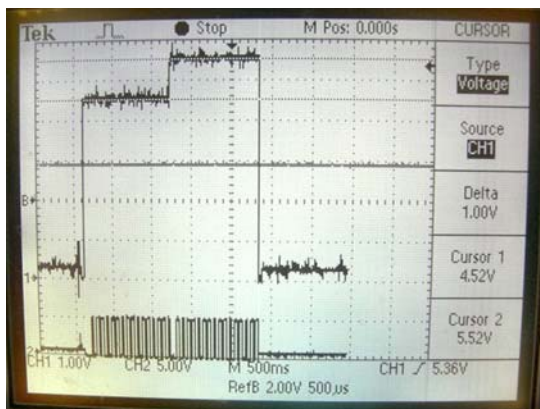


**Figure 1.**  
 $V_{CC}$  held at 5.0 V through the test sequence  
– should be at 4.5 and 5.5 V.

When we repeated these same tests using the Unisite Data I/O we found 100% compliance to the specification. See Figure 2 showing  $V_{CC}$  at both 4.5 and 5.5 V.

This nonconformity of the ALL-11 programmer to the specification is most surprising and disturbing as well. As noted, the programming spec requires 2 verification flows; one at  $V_{CC} = 4.5V$  and a second at  $V_{CC} = 5.5V$ , which ensures that all address locations pass with some margin. This is done because the programmable cell threshold voltage ( $V_t$ ) may have some variation after programming the entire array due to a "disturb" phenomenon. Any memory cell will deviate slightly from its initial programmed value. The low/high  $V_{CC}$  test flow is to reject parts with cell deviations of a magnitude that the charge is insufficient to pass at the  $V_{CC}$  extremes, which are +/- 10% of the 5 V  $V_{CC}$  device spec.

As noted, we have empirically determined that the ALL-11 verifies the programmed part only at  $V_{CC} = 5V$  and thus does not provide for any margin from the typical value of 5V. In cases where the  $V_t$  is close to the margin and the cell is not well programmed (due to the "disturb") it is highly likely that the cell may lose programmed data over time. Indeed this is not acceptable even for commercial parts and certainly not for MIL grade parts requiring higher reliability.

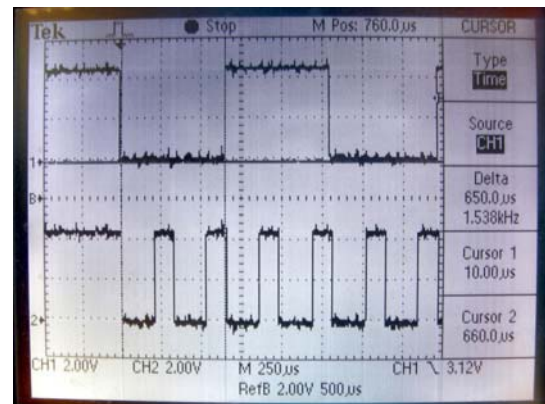


**Figure 2.**  
Data I/O  $V_{CC}$  at both 4.5 and 5.5 V.

**Timing Pulse Discrepancies:** From the programming spec for the 7C261 we note that there are at least two programming pulses required. The spec notes that when the first programming pulse is "verified" as passed, there will be an extra programming pulse with pulse width equal to about 4 times the first programming pulse. That is, the "minimum" program event happens within a single

address cycle, which is about 2 programming pulses. This is followed with a second pulse about 4X the duration of the first pulse. The extra 4X programming pulse is specified so as to increase the programmed EPROM cell  $V_t$  margin, to make it robust in the face of the "program disturb" which may occur during subsequent programming of the whole array, as well as the higher  $V_{CC}$  verification at the end of the test sequence.

On the ALL-11 we measured address bit changes related to the program pulses. The results in Figure 3 show that there are two 200ms pulses for each address. In the screen shot we can observe that on the ALL-11  $T_{pp}$  is around 200ms, which meets the minimum time of the programming specifications. The other timing looks fine such as the Verify width at 12ms. So on the ALL-11 there is a single Program pulse and a single Verify pulse. The screen shot the second PGMB pulse width of ALL-11 programmer is not 4X of the first PGMB pulse, which is required per the spec. Additionally, in Figure 4 below we can see additional not to spec performance of the observed ALL-11.



**Figure 3.**  
ALL-11 PGMB pulses, not to spec.

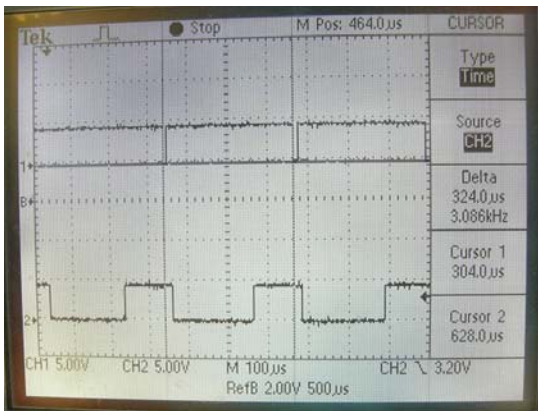
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## Programming and Verify Problems

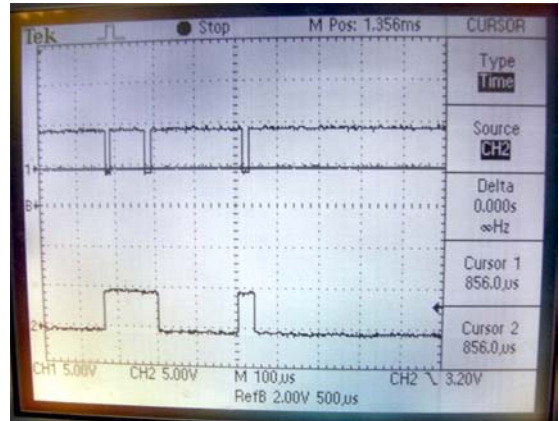
### Programmer Recommendation

These results are different from the programming specification and from the observed waveforms of the Unisite Data I/O as shown in Figure 5 below, which is a screen capture of the Data I/O waveforms, for the same programming activity. We see that in programming one word, there are 2 Program pulses and 3 Verify pulses. The first program pulse is around 200ms which is similar to the ALL-11 time. However, one can clearly see that the second is a longer 750ms program pulse.

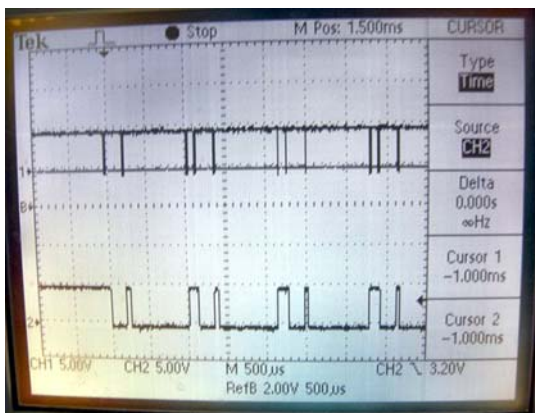
Figure 6 shows a zoom-in of Figure 5, again compare the number of program and verify pulses between the Data I/O and the ALL-11.



**Figure 4.**  
ALL-11 Zoomed PGMB, not to spec



**Figure 6.**  
Zoom-in on Data I/O correct program pulses

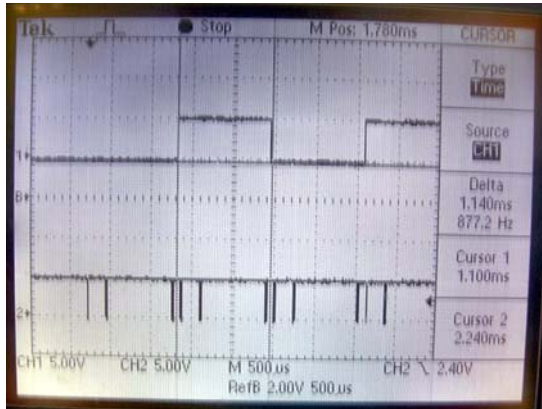


**Figure 5.**  
ALL-11 Zoomed PGMB, not to spec



**Figure 7.**  
Data I/O A0 Program - showing LSB address pin and Pgm pulse

Figure 8 clearly shows 3 verify pulses per address location.



**Figure 8.**  
Data I/O Program/Verify

So the screen shot sequence of the Data I/O program/verify timing, which aligns with the specifications, is as follows:

Address latch → Verify → Short Programming → Verify → Long Programming → Verify → next address and repeat

While the ALL-11 is observed to utilize the following abridged sequence:

Address latch → Short Programming → Verify → Short Programming → Verify → next address and repeat

### Conclusion

QP Semiconductor highly recommends that customers programming either the Cypress or QP UV PROMS only use the Unisite Data I/O and avoid ALL-11 & similar programmers due to a real possibility of field failure due to improper programming.

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