Generic I Programming Procedures

The Signetics family of Schottky PROMs are high performance bipolar devices which use a nickel/chromium (nichrome) alloy fuse to provide the many benefits of field programming. All Signetics Schottky PROMs use a common fuse design and programming circuitry. This means that a programmer capable of programming any Signetics PROM should program the entire family. Because of the pinout variation a small selection of socket adapters may be required. Programming is accomplished by application of voltages above those used for normal operation, therefore, no special pins are required for programming (except the 82S115 which has two pins: FE1 and FE2). The programming voltages and timing requirements make unintentional programming virtually impossible. Arrays of devices may be programmed in the users circuit, it desirable, and isolation of programming voltages is provided.

Signetics encourages the purchase of programming equipment from a manufacturer who has a full line of programming products to otter. Signetics also encourages the manutacuturers of PROM programming equipment to submit their equipment for veritication of electrical parameters and programming procedures. Information on manufacturers equipment is available on request from Bipolar Memory Marketing.

In order to consistently achieve excellent programming yields, periodic calibration of the programming equipment is required. Consult the equipment manufacturer for the recommended calibration interval. Records of programming yield, by device type, should be kept and any downward trend or sudden change should be considered as an indication of a need to recalibrate programming equipment.

The following information is provided for reference and completeness of individual data sheets.

SIGNETICS DISCOURAGES THE CONSTRUCTION AND USE OF "HOMEMADE" PROGRAMMING EQUIPMENT.

The generic family of Schottky PROMs uses no special pins for programming. The programming mode is evoked by raising the Vcc pin to +8.76 +/- .25V. This voltage is referred to as Vccp. The address pins remain TTL compatible and are used to address the unique word to be programmed. The outputs are used to supply fusing current in the programming mode.

Programming is performed one bit at a time, the word address is set up on the address inputs and the fuse to be programmed is selected by raising the output (corresponding to the bit in the word) to + 17V +/- 1 V. This voltage is known as Vopf and must be supplied by a voltage source with a low impedance and very test transient response. Reliable programming depends on the Vopf power supply and circuitry. Iopf is the current which should be drawn by the part during the programming sequence VOPF should be maintained and Vopf monitored. If the current is not within specification reliable fusing can not be assured.

Unprogrammed parts are supplied with all bits "zero", only the bits Intended to be "one" will be programmed.

PROGRAMMING SYSTEM SPECIFICATIONS[4] (Testing of these limits may cause programming of device.) T_A = +25°C

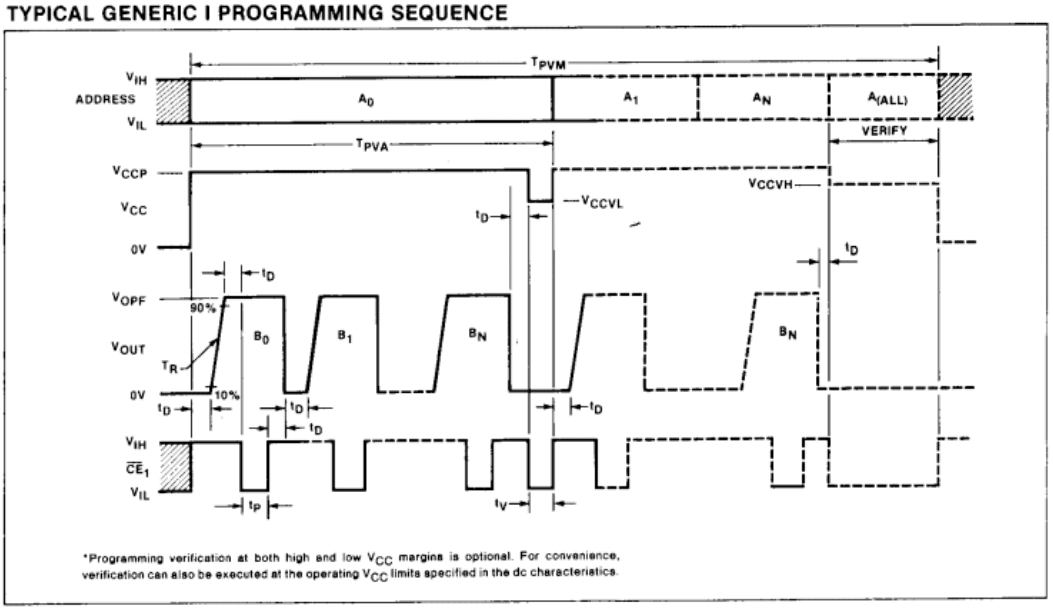
PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Rec	LIMITS Max	UNIT
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 425 + 75mA, Transient or steady state	8.5	8.75	9.0	V
	Verify limit					V
V_{CCVH}	Upper		5.3	5.0	5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					µA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			−500	
V_{OPF}	Forced output voltage (program)[3]	I_{OPF} = 200 ± 20mA, Transient or steady state	17	17.5	18.0	V
I_{OPF}	Forced output current (program)	V_{OPF} = +17 ± 1V	180		220	mA
T_{RZ}	Output pulse rise time		17	20	25	µs
t_P	$\overline{CE}$ programming pulse width		10	10	25	µs
t_D	Pulse sequence delay		5	/0		µs
T_V	$\overline{CE}$ verify pulse width		1			µs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01µF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/µs, and 10µs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment. Programming procedure for devices not listed in table 1 are found with the device data sheet.

A fuse which does not blow during the first programming cycle should be considered a defective device and should be discarded. Verification of the device may be performed after all addresses have bean programmed.

TYPICAL GENERIC I PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

PROGRAMMING PROCEDURE

- 1. Terminate all device outputs with a 10kOhm resistor to Vcc (10K resistor is the pullup resistor for open collector devices).

- 1. Terminate all device outputs with a 10KOhm resistor to Vcc (10K resistor is the pullup resistor for open collector devices).
- 2. Consult table 1 for CE conditions.
- 3. Select the Address to be programmed and raise Vcc to VCCP
- 4. Atter Td delay, apply Vopf to the output to be programmed. Program one output at the time. Note leading edge rise time restrictions.
- 5. After Td delay, pulse the /CEx input to logic low for a time tp.
- 6. After Td delay, remove Vopf from the programmed output.
- 7. Repeat steps 4 through 6 to program other bits at the same address.
- 8. To verity programming of all bite at the same address, after Td delay lower VCC to Vccvl and apply a logic low level to the /CEx input. All programmed outputs should remain in the logic high state.
- 9. After Td delay, repeat steps 3 through 8 to program and verity all other address locations.
- 10. After Td delay, raise Vcc to VCCVH and verity all memory locations by applying a logic low level to /CEx and cycling through all device addresses.

GENERIC 11 PROGRAMMING PROCEDURE

The programming procedure for fusing the oxide-isolated vertical fuse PROMs is under development, and is not available at the time of printing. Please contact the factory for details on the Generic 11 programming method.